Abstract of the Disclosure

A semiconductor memory device having a uniform bit line sensing margin time independent on an external voltage variation, includes: a memory cell coupled to a bit line and a word line; an amplifier for amplifying an electric potential of the bit line; a first control signal generator to which an external voltage is supplied for activating the word line; and a second control signal generator to which a core voltage is supplied for controlling an execution of the amplifier by receiving the first control signal.